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CAT25010, CAT25020, CAT25040

1K/2K/4K SPI Serial CMOS EEPROM

FEATURES

- 10 MHz SPI compatible
- 1.8 to 5.5 volt operation
- SPI modes (00 & 11)
- 16-byte page write buffer
- Self-timed write cycle
- Hardware and software protection
- Block write protection
  – Protect 1/4, 1/2 or all of EEPROM array
- Low power CMOS technology
- 1,000,000 program/erase cycles
- 100 year data retention
- Industrial temperature range
- RoHS-compliant 8-lead PDIP, SOIC, TSSOP and 8-pad TDFN packages.

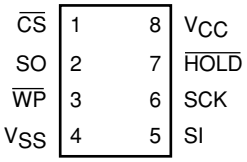
For Ordering Information details, see page 17.

DESCRIPTION

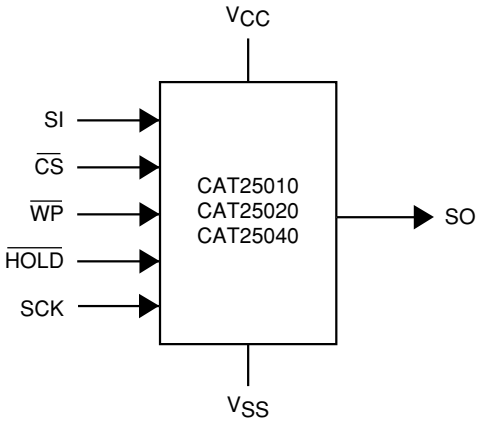
The CAT25010/20/40 is a 1K/2K/4K Bit SPI Serial CMOS EEPROM internally organized as 128x8/256x8/512x8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25010/20/40 features a 16-byte page write buffer. The device operates via the SPI bus serial interface and is enabled though a Chip Select ($\overline{CS}$). The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25010/20/40 is designed with software and hardware write protection features including Block Write protection.

PIN CONFIGURATION

PDIP (L)
SOIC (V)
TSSOP (Y)
TDFN (VP2)



FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
$\overline{WP}$	Write Protect
V_{CC}	+1.8V to +5.5V Power Supply
V_{SS}	Ground
$\overline{CS}$	Chip Select
SI	Serial Data Input
$\overline{HOLD}$	Suspends Serial Input

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Doc. No. 1006, Rev. S

ABSOLUTE MAXIMUM RATINGS(1)

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground(2)	-0.5 V to +6.5 V

RELIABILITY CHARACTERISTICS(3)

Symbol	Parameter	Min	Units
N_{END}(4)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Supply Current	Read, Write, V_{CC} = 5.0V, f_{SCK} = 10MHz, SO open		2	mA
I_{SB1}	Standby Current	V_{IN} = GND or V_{CC}, $\overline{CS}$ = V_{CC}, $\overline{WP}$ = V_{CC}, V_{CC} = 5V		2	µA
I_{SB2}	Standby Current	V_{IN} = GND or V_{CC}, $\overline{CS}$ = V_{CC}, $\overline{WP}$ = GND, V_{CC} = 5V		4	µA
I_L	Input Leakage Current	V_{IN} = GND or V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{CC}, V_{OUT} = GND or V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} > 2.5V, I_{OL} = 3.0mA		0.4	V
V_{OH1}	Output High Voltage	V_{CC} > 2.5V, I_{OH} = -1.6mA	V_{CC} - 0.8V		V
V_{OL2}	Output Low Voltage	V_{CC} > 1.8V, I_{OL} = 150µA		0.2	V
V_{OH2}	Output High Voltage	V_{CC} > 1.8V, I_{OH} = -100µA	V_{CC} - 0.2V		V

PIN CAPACITANCE(3)

T_A = 25°C, f = 1 MHz, V_{CC} = 5V

Symbol	Test Conditions	Max	Conditions	Units
C_{OUT}	Output Capacitance (SO)	8	V_{OUT} = 0 V	pF
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	V_{IN} = 0 V	pF

Note:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5V or higher than V_{CC} + 0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5V, for periods of less than 20ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5 V, 25°C

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A.C. CHARACTERISTICS

T_A = -40°C to +85°C, unless otherwise specified.(1)

SYMBOL	PARAMETER	V_{CC} = 1.8V-5.5V		V_{CC} = 2.5V-5.5V		UNITS
		Min.	Max.	Min.	Max.	
t_{SU}	Data Setup Time	30		20		ns
t_H	Data Hold Time	30		20		ns
t_{WH}	SCK High Time	75		40		ns
t_{WL}	SCK Low Time	75		40		ns
f_{SCK}	Clock Frequency	DC	5	DC	10	MHz
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		25	ns
t_{RI}(2)	Input Rise Time		2		2	µs
t_{FI}(2)	Input Fall Time		2		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	0		0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		10		ns
t_{WC}(4)	Write Cycle Time		5		5	ms
t_V	Output Valid from Clock Low		75		40	ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		50		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		100		25	ns
t_{CS}	$\overline{CS}$ High Time	50		15		ns
t_{CSS}	$\overline{CS}$ Setup Time	50		15		ns
t_{CSH}	$\overline{CS}$ Hold Time	50		15		ns
t_{WPS}	$\overline{WP}$ Setup Time	10		10		ns
t_{WPH}	$\overline{WP}$ Hold Time	10		10		ns

Power-Up Timing(2)(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

NOTE:
(1) AC Test Conditions:
Input Pulse Voltages: 0.3V_{CC} to 0.7V_{CC}
Input rise and fall times: ≤10ns
Input and output reference voltages: 0.5V_{CC}
Output load: current source IOL max/IOH max; C_L=50pF
(2) This parameter is tested initially and after a design or process change that affects the parameter.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

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FUNCTIONAL DESCRIPTION

The CAT25010/20/40 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25010/20/40 to interface directly with many of today's popular microcontrollers. The CAT25010/20/40 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

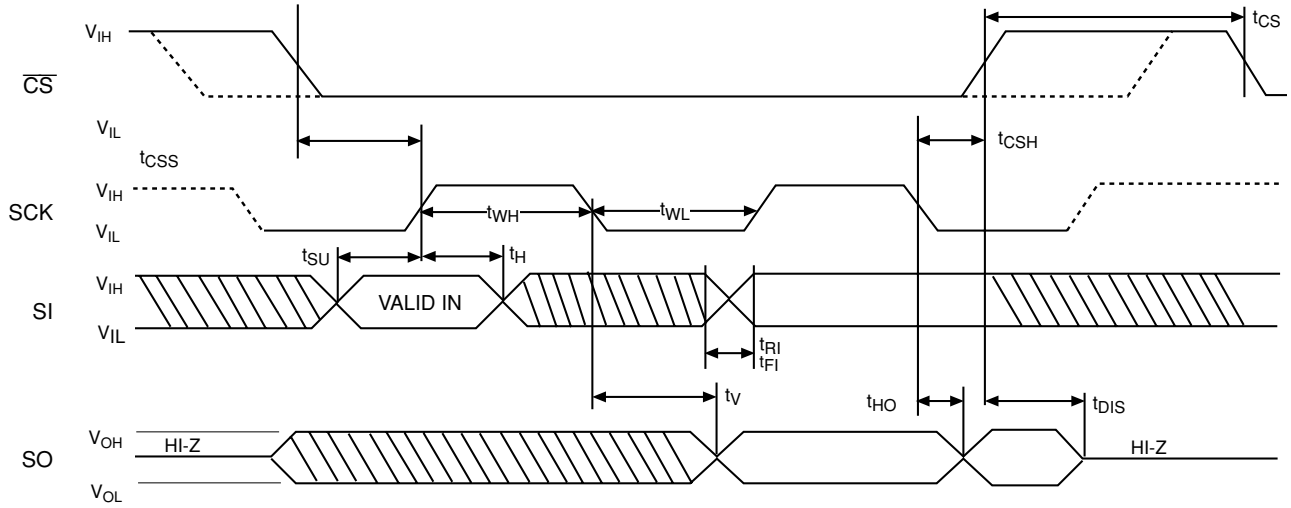
After the device is selected with $\overline{CS}$ going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

PIN DESCRIPTION

SI: Serial Input
SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the CAT25010/20/40. Input data is latched on the rising edge of the serial clock for SPI modes (0, 0 & 1, 1).

SO: Serial Output
SO is the serial data output pin. This pin is used to transfer data out of the CAT25010/20/40. During a read cycle, data is shifted out on the falling edge of the serial clock for SPI modes (0,0 & 1,1).

Figure 1. Sychronous Data Timing



Note: Dashed Line= mode (1, 1) – – – – –

INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 X011(1)	Read Data from Memory
WRITE	0000 X010(1)	Write Data to Memory

Note:
(1) X=0 for CAT25010, CAT25020. X=A8 for CAT25040

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SCK: Serial Clock
SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the CAT25010/20/40. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK for SPI modes (0,0 & 1,1) .

$\overline{CS}$: Chip Select
$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the CAT25010/20/40 and $\overline{CS}$ high disables the CAT25010/20/40. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect
$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low all write operations are inhibited. $\overline{WP}$ held low while $\overline{CS}$ is low will interrupt a write to the CAT25010/20/40. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation. Figure 10 illustrates the $\overline{WP}$ timing sequence during a write operation.

$\overline{HOLD}$: Hold
The $\overline{HOLD}$ pin is used to pause transmission to the CAT25010/20/40 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{CC} or tied to V_{CC} through a resistor. Figure 9 illustrates hold timing sequence.

STATUS REGISTER

7	6	5	4	3	2	1	0
1	1	1	1	BP1	BP0	WEL	$\overline{RDY}$

BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	CAT25010: 60-7F CAT25020: C0-FF CAT25040: 180-1FF	Quarter Array Protection
1	0	CAT25010: 40-7F CAT25020: 80-FF CAT25040: 100-1FF	Half Array Protection
1	1	CAT25010: 00-7F CAT25020: 00-FF CAT25040: 000-1FF	Full Array Protection

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STATUS REGISTER

The Status Register indicates the status of the device. The $\overline{RDY}$ (Ready) bit indicates whether the CAT25010/20/40 is busy with a write operation. When set to 1 a write cycle is in progress and when set to 0 the device indicates it is ready. This bit is read only.

The WEL (Write Enable) bit indicates the status of the write enable latch. When set to 1, the device is in a Write Enable state and when set to 0 the device is in a Write Disable state. The WEL bit can only be set by the WREN instruction and can be reset by the WRDI instruction.

The BP0 and BP1 (Block Protect) bits indicate which blocks are currently protected. These bits are set by the user issuing the WRSR instruction. The user is allowed to protect quarter of the memory, half of the memory or the entire memory by setting these bits. Once protected, the user may only read from the protected portion of the array. These bits are non-volatile.

DEVICE OPERATION

Write Enable and Disable

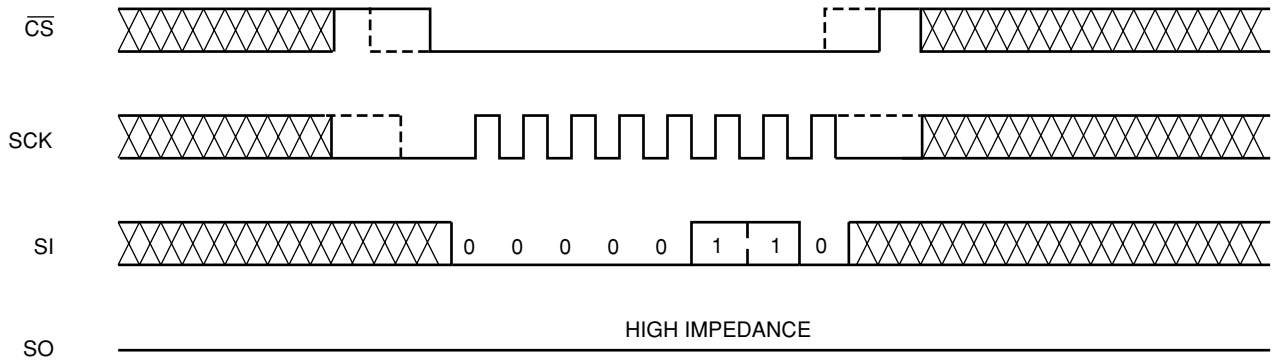
The CAT25010/20/40 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when V_{CC} is applied. WREN instruction will enable writes (set the latch) to the device. If $\overline{WP}$ pin is held low, the write enable latch is reset to the write disabe state, regardless of the WREN Instruction. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

READ Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the CAT25010/20/40, followed by the 8-bit address for CAT25010/20/40 (for the 25040, bit 3 of the read data instruction contains address A8).

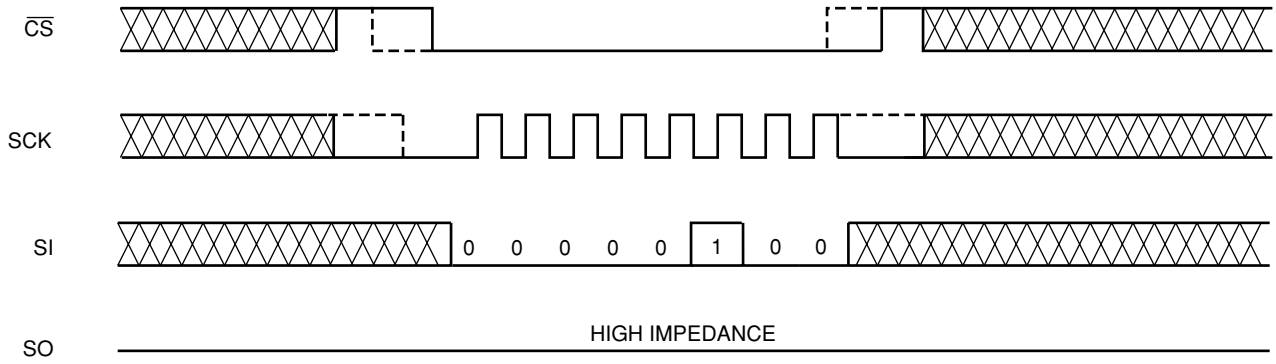
After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing

Figure 2. WREN Instruction Timing



Note: Dashed Line = mode (1, 1) – – – – –

Figure 3. WRDI Instruction Timing



Note: Dashed Line = mode (1, 1) – – – – –

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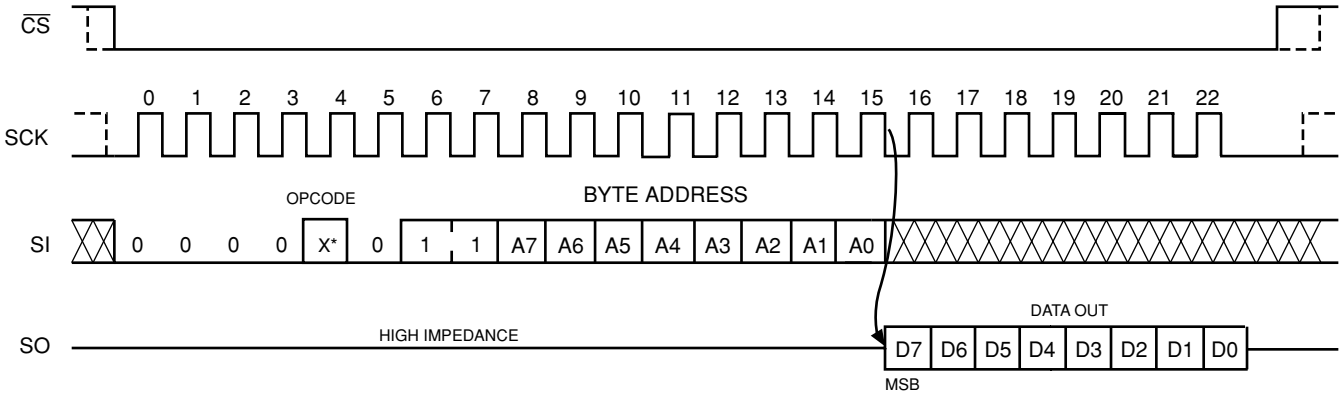
to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the $\overline{CS}$ high. Read sequece is illustrated in Figure 4.

To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. The status register may be read at any time even during a write cycle. Reading status register is illustrated in Figure 5.

WRITE Sequence

The CAT25010/20/40 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25010/20/40. The device goes into Write enable state by pulling the $\overline{CS}$ low and then clocking the WREN instruction into CAT25010/20/40. The $\overline{CS}$ must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the

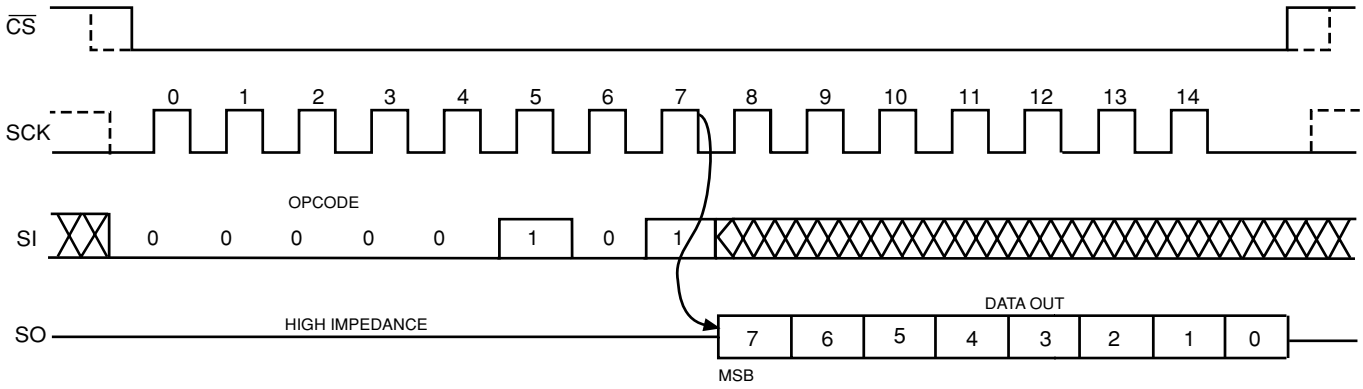
Figure 4. Read Instruction Timing


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
OPCODE
BYTE ADDRESS
SI
0 0 0 0 X* 0 1 1 A7 A6 A5 A4 A3 A2 A1 A0
DATA OUT
SO
HIGH IMPEDANCE
D7 D6 D5 D4 D3 D2 D1 D0
MSB

*Please check the instruction set table for address
X=0 for 25010, 25020 ; X=A8 for 25040

Note: Dashed line = mode (1,1)----

Figure 5. RDSR Instruction Timing



Note: Dashed Line= mode (1, 1) – – – – –

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address of the memory location(s) to be programmed must be outside the protected address field location selected by the block protection level.

Byte Write

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the $\overline{CS}$ low, issuing a write instruction via the SI line, followed by the 8-bit address for 25010/20/40 (for the 25040, bit 3 of the read data instruction contains address A8). Programming will start after the $\overline{CS}$ is brought high. Figure 6 illustrates byte write sequence.

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction

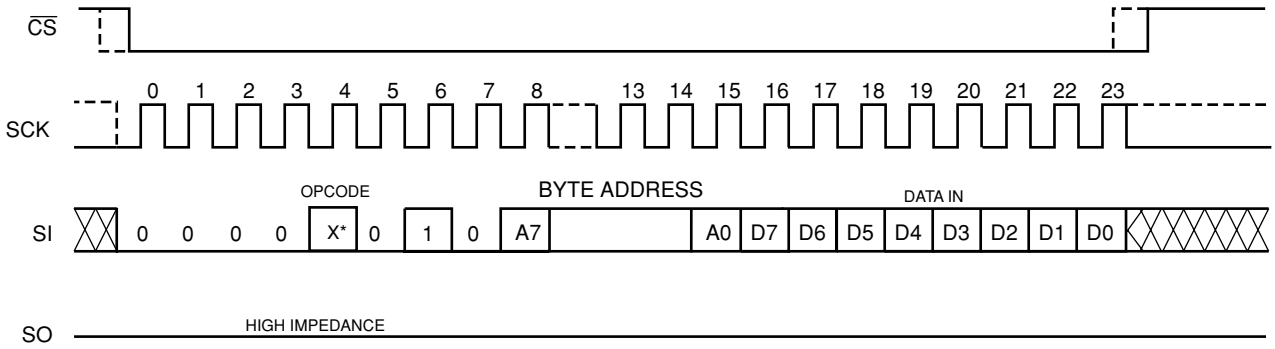
Page Write

The CAT25010/20/40 features page write capability. After the initial byte, the host may continue to write up to 16 bytes of data to the CAT25010/20/40. After each byte of data received, lower order address bits are internally incremented by one; the high order bits of address will remain constant. The only restriction is that the X (X=16 for CAT25010/20/40) bytes must reside on the same page. If the address counter reaches the end of the page and clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written. The CAT25010/20/40 is automatically returned to the write disable state at the completion of the write cycle. Figure 8 illustrates the page write sequence.

Status Register Write

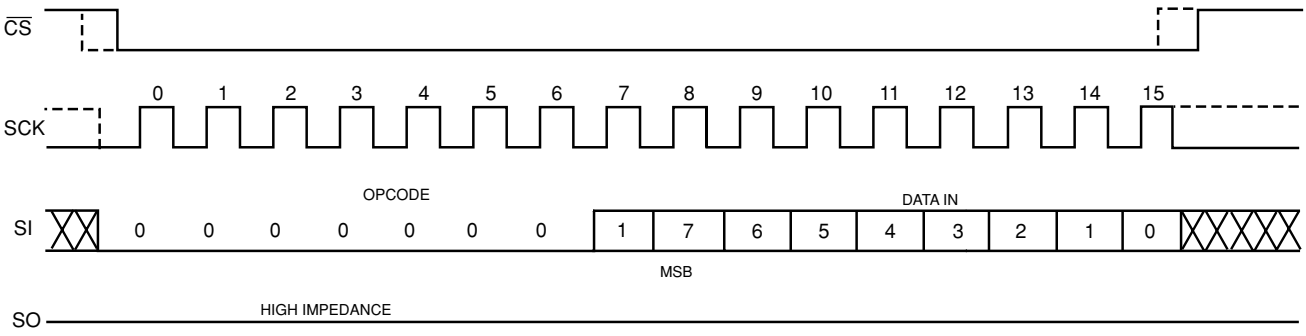
To write to the status register, the WRSR instruction should be sent. Only Bit 2 and Bit 3 of the status register can be written using the WRSR instruction. Figure 7 illustrates the sequence of writing to status register.

Figure 6. Write Instruction Timing


CS
SCK
0 1 2 3 4 5 6 7 8 13 14 15 16 17 18 19 20 21 22 23
SI
OPCODE
BYTE ADDRESS
DATA IN
0 0 0 0 X* 0 1 0 A7 A0 D7 D6 D5 D4 D3 D2 D1 D0
SO
HIGH IMPEDANCE

Note: Dashed Line= mode (1, 1) – – – – –
*X=0 for 25010, 25020 ; X=A8 for 25040

Figure 7. WRSR Timing



Note: Dashed Line= mode (1, 1) – – – – –

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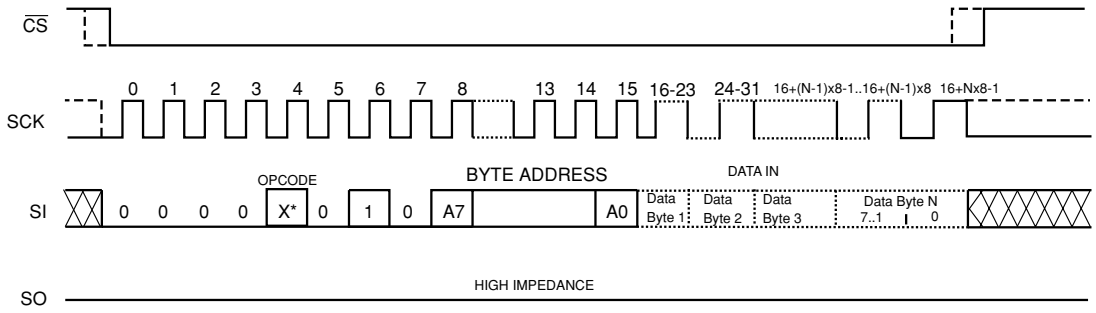
DESIGN CONSIDERATIONS

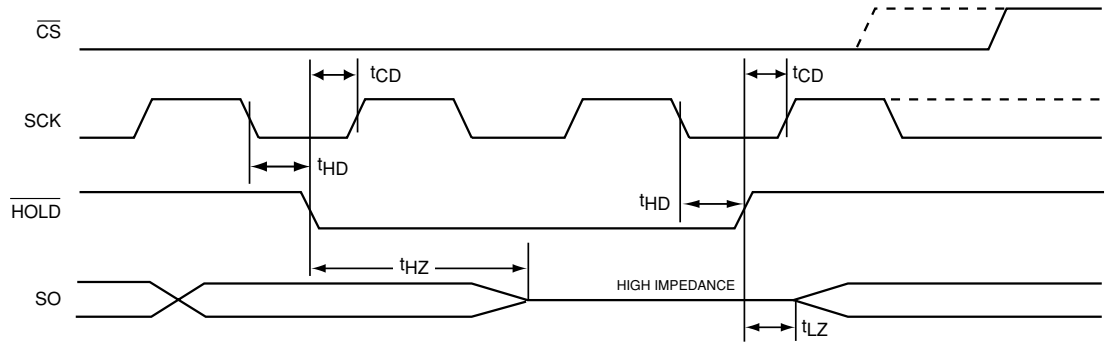
The CAT25010/20/40 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued to perform any writes to the device after power up. After power up, $\overline{CS}$ must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the CAT25010/20/40 goes into a write disable mode. $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and programming is continued. On power up, SO is in a high impedance. If an invalid opcode is received, no data will be shifted into the CAT25010/20/40, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again.

Figure 8. Page Write Instruction Timing



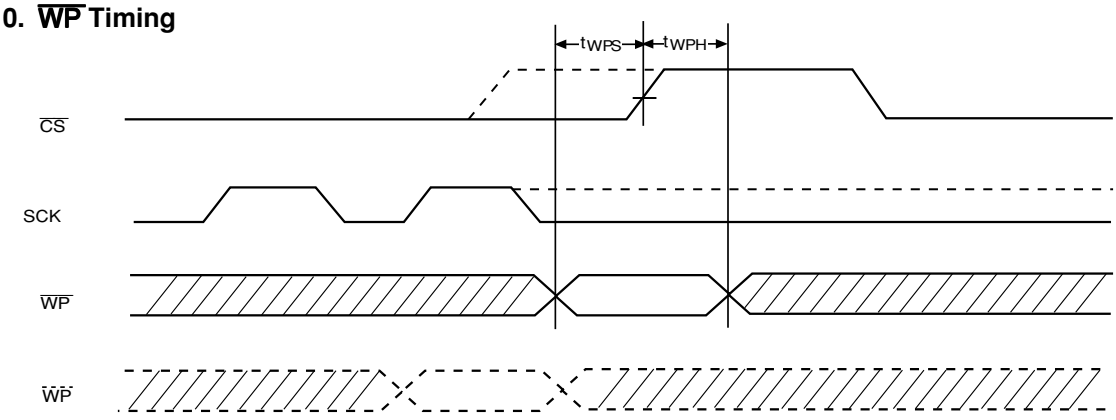
Note: Dashed Line= mode (1, 1) – – – – – *X=0 for 25010, 25020 ; X=A8 for 25040

Figure 9. $\overline{HOLD}$ Timing



Note: Dashed Line= mode (1, 1) – – – – –

Figure 10. $\overline{WP}$ Timing



Note: Dashed Line= mode (1, 1) – – – – –

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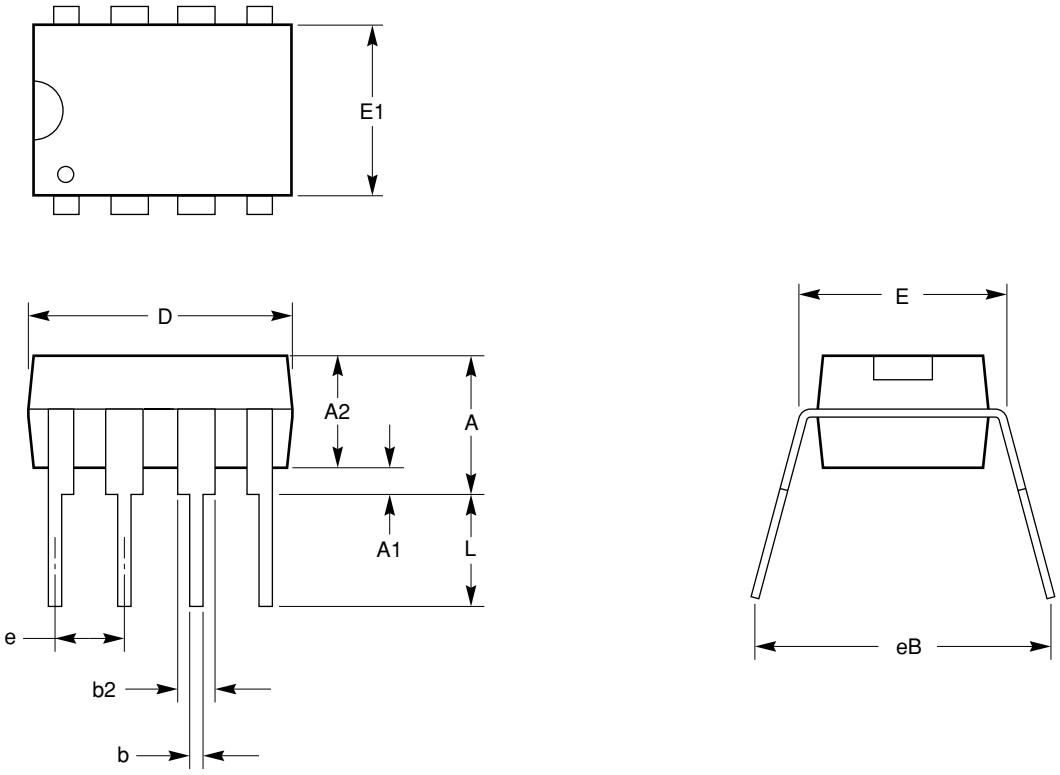
8-LEAD 300 MIL WIDE PLASTIC DIP (L)



SYMBOL	MIN	NOM	MAX
A			4.57
A1	0.38		
A2	3.05		3.81
b	0.36	0.46	0.56
b2	1.14		1.77
D	9.02		10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54 BSC	
eB	7.87		9.65
L	0.115	0.130	0.150

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MS001.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

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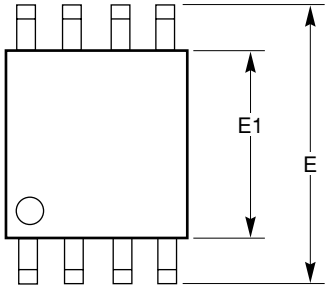
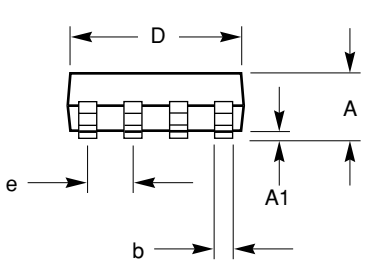
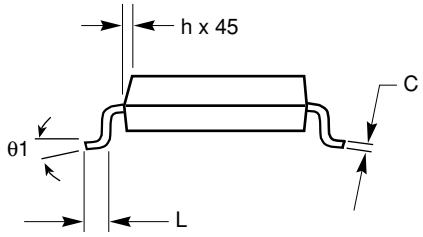
8-LEAD 150 MIL WIDE SOIC (V)







SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-012.

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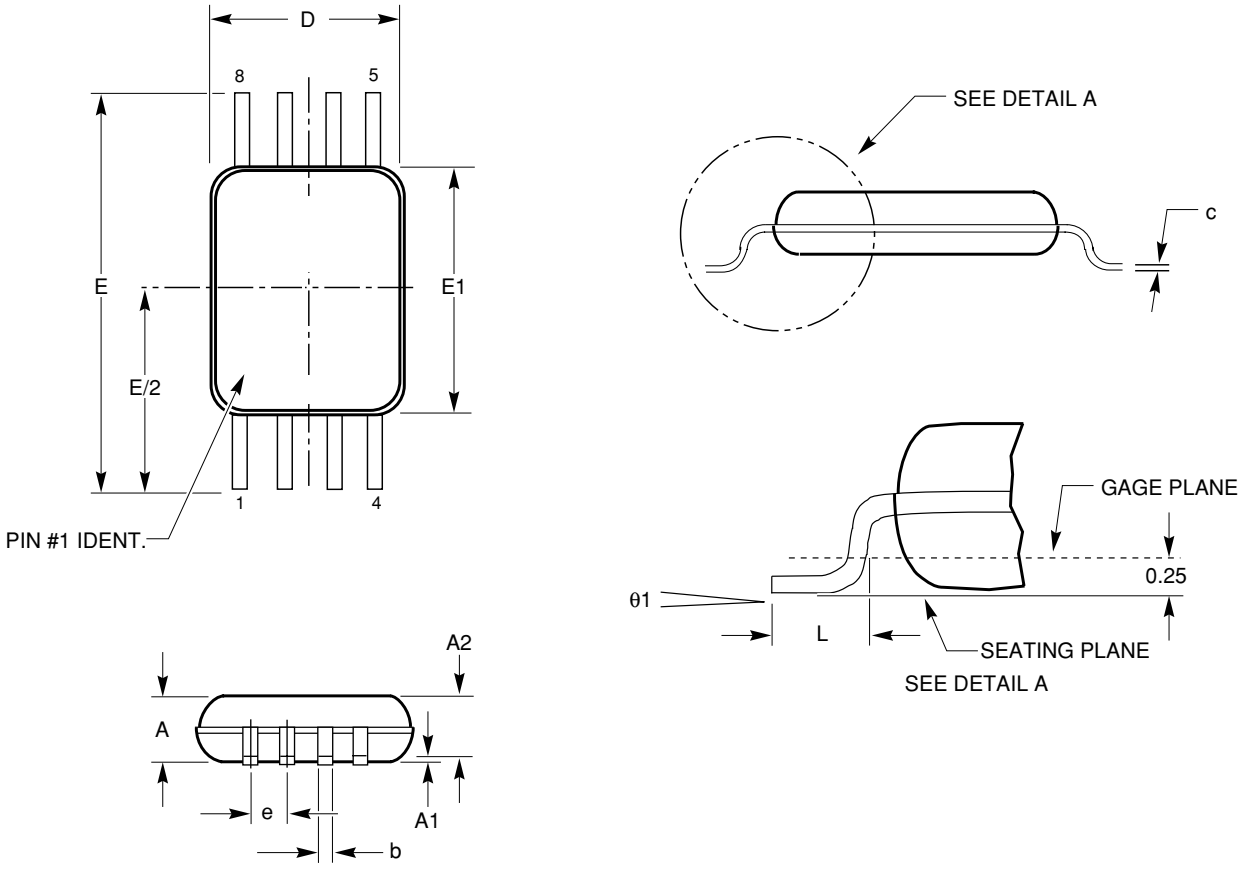
8-LEAD TSSOP (Y)



SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
θ1	0.00		8.00

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MO-153

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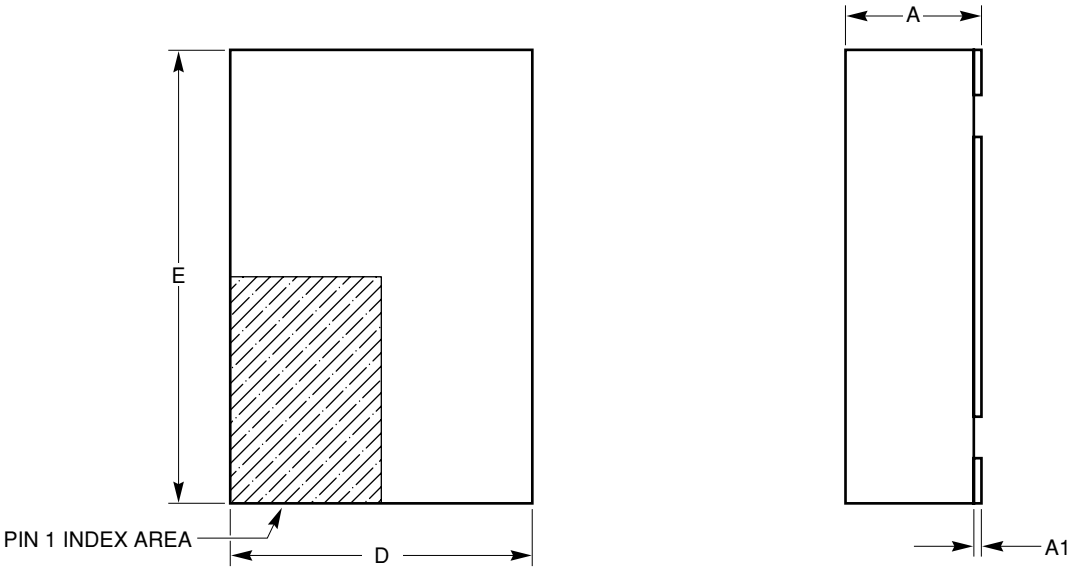
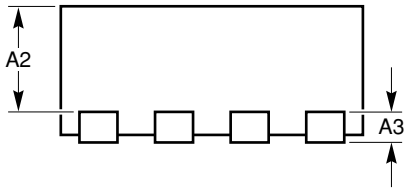
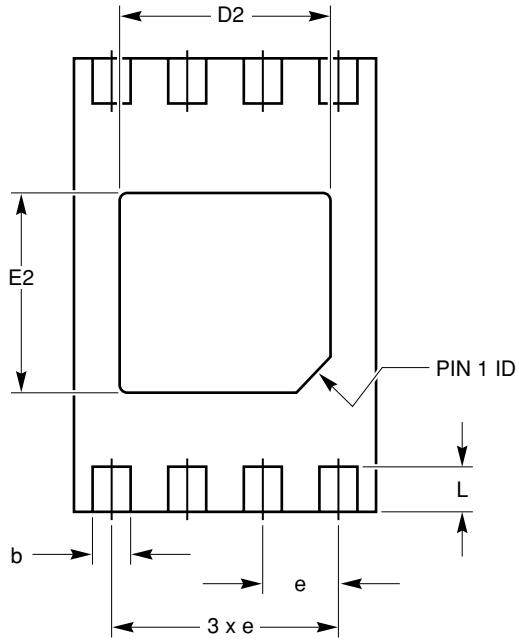
8-PAD TDFN 2X3 PACKAGE (VP2)





SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40



For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

TDFN2X3 (03).eps

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MO-229

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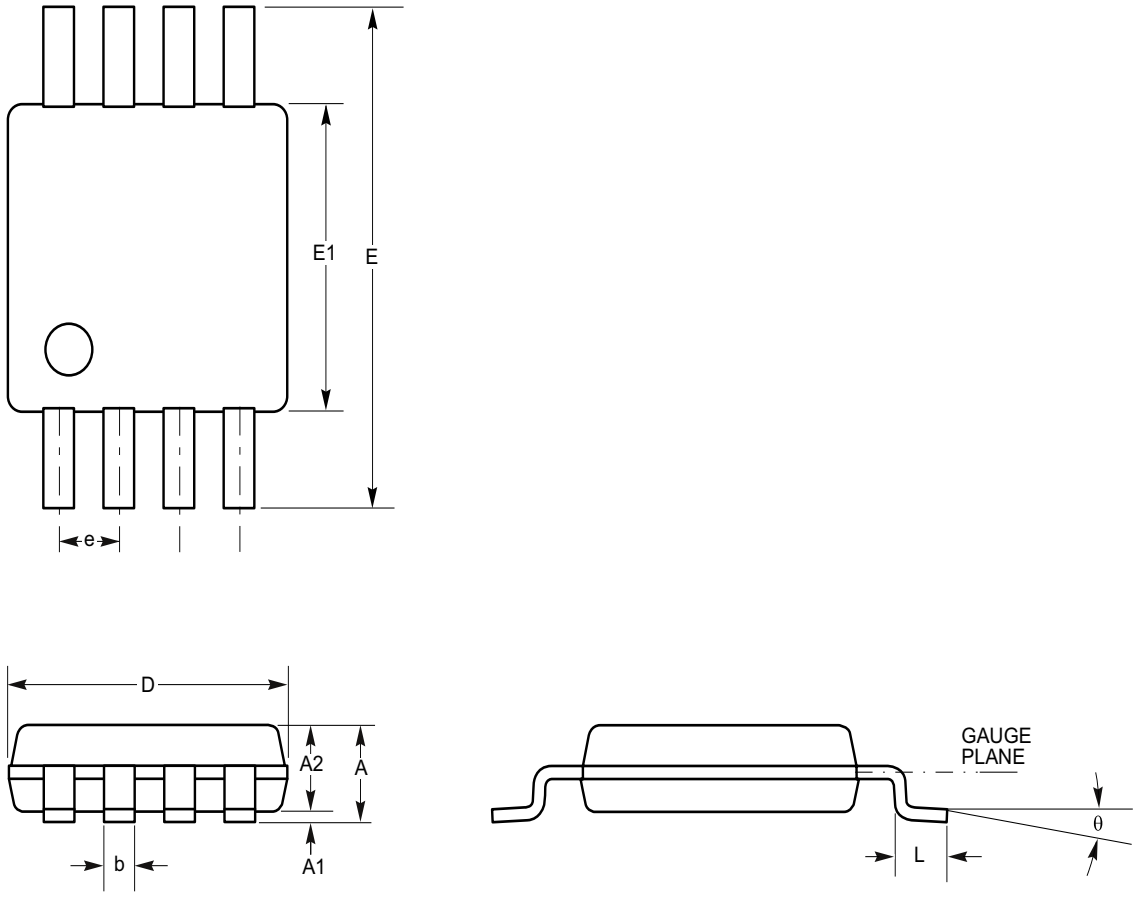
8 LEAD MSOP (Z)



SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.00		0.15
A2	0.75		0.95
b	0.22		0.38
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40		0.8
θ	0°		8°

8-lead_MSOP3.eps

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Specification MO-187.
3. Stand off height/coplanarity are considered as special characteristics.

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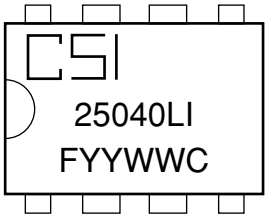
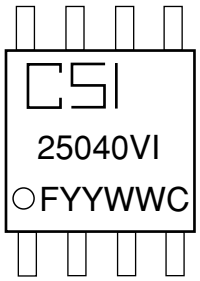
PACKAGE MARKING

8-Lead PDIP



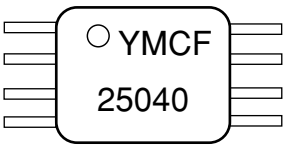
CSI = Catalyst Semiconductor, Inc.
25040L = Device Code:
25010L
25020L
25040L
I = Temperature Range
YY = Production Year
WW = Production Week
C = Product Revision
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead SOIC



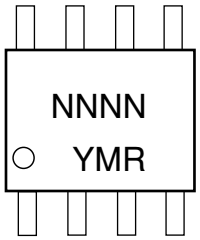
CSI = Catalyst Semiconductor, Inc.
25040V = Device Code:
25010V
25020V
25040V
I = Temperature Range
YY = Production Year
WW = Production Week
C = Product Revision
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead TSSOP



Y = Production Year
M = Production Month
C = Product Revision
25040 = Device Code:
25010
25020
25040
I = Industrial Temperature Range
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead MSOP



NNNN =	Device Code	
	Matte Tin	NiPdAu
25010	ABPH	ABPJ
25020	ABPF	ABKP
25040	ABPG	ABCY

Y = Production Year
M = Production Month
C = Production Revision

Notes:
(1) The circle on the package marking indicates the location of Pin 1.

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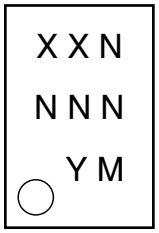
8-Pad TDFN (2x3mm)



XX = Device Code

	Matte-Tin	NiPdAu
25010	FH	FG
25020	FE	FC
25040	FF	FD

N = Traceability Code
Y = Production Year
M = Production Month

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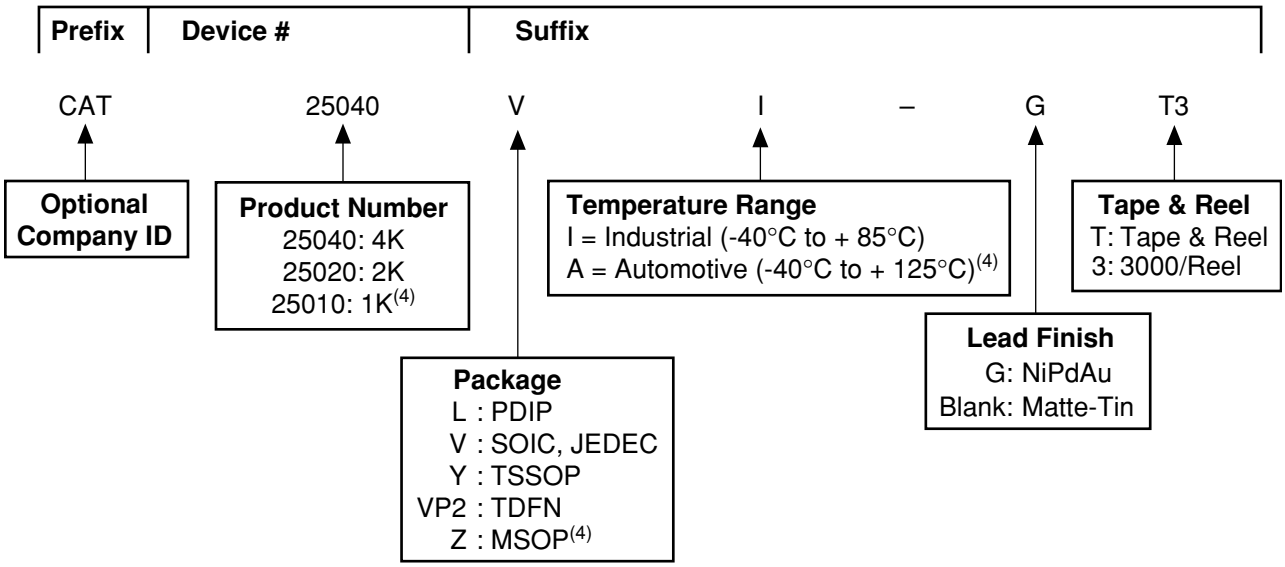
EXAMPLE OF ORDERING INFORMATION



Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu.
(3) The device used in the above example is a CAT25040VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).
(4) For availability, please contact your nearest Catalyst Semiconductor Sales office.

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REVISION HISTORY

Date	Rev.	Reason
10/13/05	N	Update D.C. Operating Characteristics Update Ordering Information
12/09/05	O	Update Pin Configuration Update D.C. Operating Characteristics Update Pin Impedance Characteristics Update Figure 2, 3, 4, 6, 8 Add Tape and Reel Update Ordering Information
03/21/06	P	Update D.C. Operating Characteristics Update A.C. Characteristics Update Pin Description
06/30/06	Q	Update Features Update Description Update A.C. Characteristics Update Package Marking Remove Tape and Reel Update Example of Ordering Information
07/31/06	R	Add TDFN and MSOP packages Update Package Marking Update Ordering Information
10/13/06	S	Update Example of Ordering Information

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Publication #: 1006
Revison: S
Issue date: 10/13/06